PHOENIX-AVSBUS

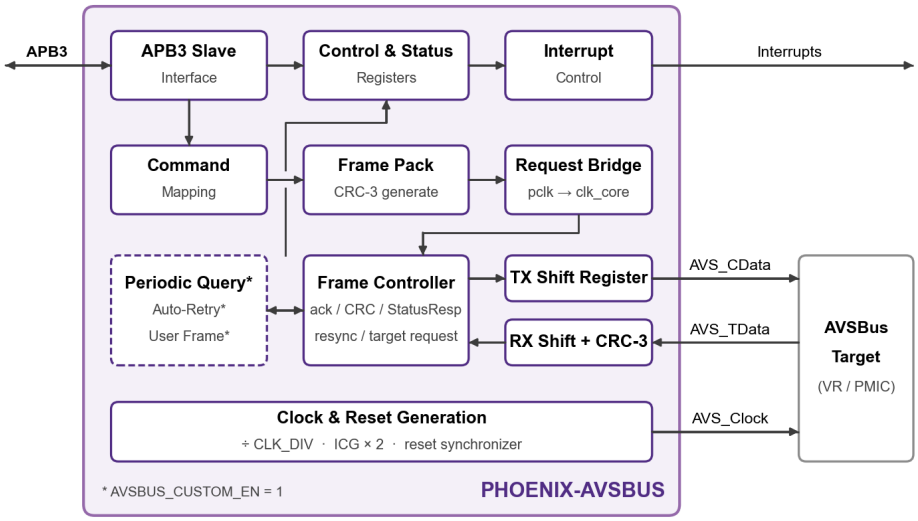
AVSBus 1.4 Controller with APB3 Host Interface

PHOENIX-AVSBUS is an AVSBus controller IP core compliant with AVSBus 1.4 (PMBus 1.4.1 Part III). It connects an SoC to AVSBus voltage regulators and PMICs over the 3-wire point-to-point interface (AVS_Clock, AVS_CData, AVS_TData) and lets software set and read rail voltage, transition rate, current, temperature, power mode and status with the low latency that adaptive voltage scaling (AVS) and DVFS control loops need.

Software controls the bus through an AMBA 3 APB slave. Each AVSBus command is started by a single APB access to a command window: the address selects the data type and the rail, a write sends a write frame and a read sends a read frame whose response is then read from a register. The core builds the controller sub-frame, generates the CRC-3, checks the acknowledge, CRC and StatusResp of every target response, captures Status Response Frames and detects target requests while the bus is idle. Every event is reported through maskable interrupt sources.

The AVSBUS_CUSTOM_EN build parameter adds optional extensions: hardware-timed periodic current and voltage queries with result ports and interrupts, automatic resynchronization and retransmission when a target does not respond, and user-defined controller sub-frames. The core runs from the single APB clock pclk: AVS_Clock is an even division of it and is parked low while the bus is idle.

Block Diagram



Implementation Results

Synthesis results with CLK_DIV = 4, timing met at pclk = 50 MHz. Standard: AVSBUS_CUSTOM_EN = 0; Custom: AVSBUS_CUSTOM_EN = 1.

Configuration	Technology	Area / Resources
Standard	TSMC 28nm HPC+	1,425 µm² · 3.8k gates
Custom	TSMC 28nm HPC+	2,473 µm² · 6.5k gates
Standard	AMD Virtex UltraScale	266 LUTs · 334 FFs
Custom	AMD Virtex UltraScale	489 LUTs · 600 FFs

ASIC: Design Compiler, ssg 0.72 V 125 °C, 1 gate = ND2D1 (0.378 µm²). FPGA: Vivado synthesis, xcvu440-3. Contact SILIPRISM for results on your target technology.

Verification

Verified in a UVM environment with APB master and AVSBus target VIP and 21 tests; the regressions pass 51/51 runs (Custom) and 38/38 runs (Standard). A directed clock-level testbench covers both configurations at CLK_DIV = 2 / 4 / 8, and the C driver is co-simulated with the RTL. Coverage: 100% functional, 97.6% or higher line, branch, condition and toggle. SpyGlass lint and CDC report no errors in either configuration.

Deliverables

- Synthesizable Verilog-2001 RTL source
- SDC constraints; Design Compiler and Vivado synthesis scripts
- SpyGlass lint and CDC setup with reviewed waivers
- UVM testbench (APB and AVSBus VIP licensed separately) and directed testbench
- C99 bare-metal driver with examples, host and co-simulation tests
- Specification, programming guide and verification guide

FEATURES

AVSBus 1.4 Compliant

- Controller for AVSBus 1.4 (PMBus 1.4.1 Part III), 3-wire mode
- All AVSBus data types: Voltage, Vout Transition Rate, Current, Temperature, Voltage Reset, Power Mode, Status, Version
- Manufacturer-specific commands (CmdGroup = 1)
- Write-and-Commit, Write-and-Hold and broadcast Select
- AVS_Clock = pclk / CLK_DIV (even, ≥ 2), up to 50 MHz, 50% duty cycle

Robust Bus Handling

- Hardware CRC-3 generation and checking
- TargetAck, StatusResp and no-response detection
- Status Response Frame capture
- Target request detection while the bus is idle
- Target resynchronization on request (34 clocks)

Easy Integration

- AMBA 3 APB slave, zero wait states
- One APB access starts an AVSBus command (memory-mapped command window)
- Up to 15 interrupt sources: W1C status, mask, software trigger, level outputs
- Single clock input (pclk), no separate AVSBus clock
- Software clock gate for low standby power
- Active-low asynchronous reset, built-in reset synchronizer for the AVS clock domain

Custom Extensions (AVSBUS_CUSTOM_EN = 1)

- Periodic current and voltage query in hardware: 16-bit interval timer, result ports and interrupts
- Automatic resync and one retransmission on no response, fatal interrupt
- User-defined 32-bit controller sub-frames

Software Support

- C99 bare-metal driver with a HAL-style API, no C library needed
- Reference examples and a programming guide

Applications

Adaptive voltage scaling and DVFS of CPU, GPU and NPU power rails; PMIC and VR control in mobile, AI, networking and server SoCs.

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