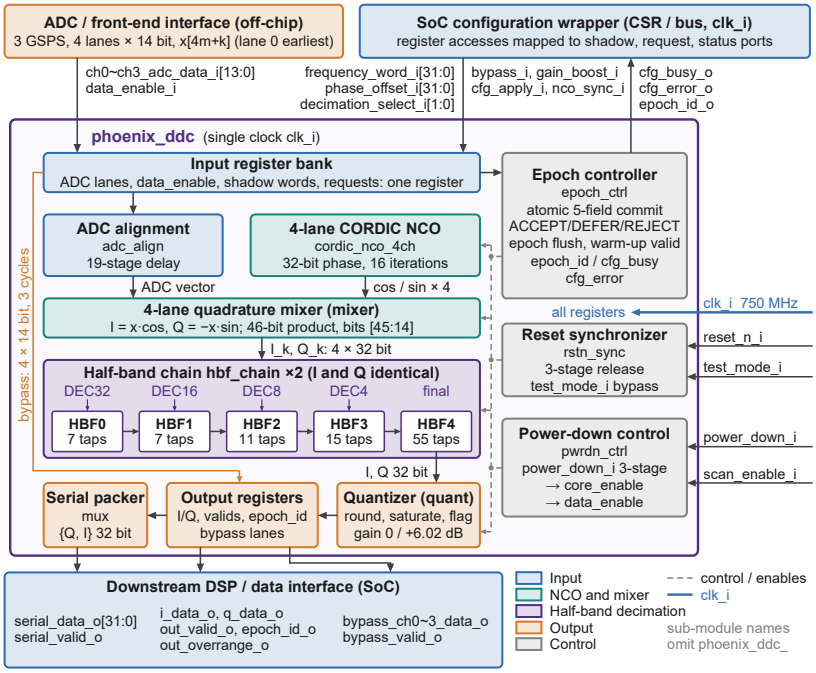
PHOENIX-DDC

3 GSPS Digital Down Converter with CORDIC NCO and Half-Band Decimation

PHOENIX-DDC is a digital down converter IP core for direct RF and IF sampling receivers. It accepts a 3 GSPS real ADC stream as four time-interleaved 14-bit lanes at 750 MHz, shifts it to complex baseband with a 32-bit NCO and a 16-iteration CORDIC quadrature mixer, and decimates by 4, 8, 16 or 32 through a five-stage half-band cascade to 16-bit complex I/Q at 750 to 93.75 MSPS. A raw ADC bypass passes the four lanes unchanged.

All ports belong to one clk_i domain. Five shadow settings (tuning word, phase word, decimation, bypass, gain) are committed atomically by a one-cycle cfg_apply_i strobe; a request is accepted, deferred to the power-down wake-up or rejected while the core is busy, and every restart carries a 4-bit epoch tag. nco_sync_i aligns the digital phase of several devices, and the first valid output follows a restart after a fixed 31 / 36 / 42 / 50 cycles.

Block Diagram



Implementation Results

Default configuration (14-bit ADC lanes, 16-bit I/Q), setup timing met at clk_i = 750 MHz.

Target	Technology	Area / Resources
ASIC	TSMC 28nm HPC+	97,075 µm² · 256.8k gates
FPGA	AMD Virtex UltraScale	22,811 LUTs · 16,076 FFs · 20 DSP

ASIC: logic synthesis, SSG 0.81 V 125 °C, pre-layout standard-cell area, setup WNS +0.000012 ns; gate count in NAND2 equivalents (0.378 µm²); no memories. FPGA: synthesis for xcvu095 at 150 MHz. Contact SILIPRISM for results on your target technology.

Verification

Verified against bit-exact fixed-point and cycle-accurate models with 145 testcases: 145/145 pass with default and 145/145 with randomized register initialization, with golden data regenerated by the model in every run, X-propagation simulation and mid-stream reset with X injected into the unreset datapath. A control scoreboard checks request arbitration, committed settings and epoch timing, and the comparator detects all 177 injected faults. Coverage: 100% functional, 98.31% line, 98.16% branch, 100.00% condition, 97.02% toggle. The synthesis netlist is proven equivalent to the RTL, the scan rule check reports 0 violations, and Lint, CDC and RDC report 0 errors.

Deliverables

- Synthesizable Verilog-2001 RTL source
- SDC constraints; ASIC and FPGA synthesis scripts
- Lint, CDC and RDC setup with rule sets and constraints
- Bit-exact fixed-point and cycle-accurate models, frequency planning
- SystemVerilog testbench, 145 testcases, scoreboards, coverage model
- Specification, programming guide with C99 parameter code, verification report

FEATURES

Input and NCO

- 3 GSPS real input: four time-interleaved 14-bit lanes at 750 MHz
- 32-bit tuning word (0.698 Hz steps) and 32-bit phase word
- 16-iteration pipelined CORDIC; LO spurs ≤ −96.10 dBc over 32 tuning words
- Quadrature mixing I = x·cos θ, Q = −x·sin θ

Decimation Filter

- DEC4 / 8 / 16 / 32: 750 / 375 / 187.5 / 93.75 MSPS I/Q
- Five linear-phase half-band stages, 7 / 7 / 11 / 15 / 55 taps
- Passband |f| ≤ 0.4·fout, ripple ≤ 0.02 dB
- Protected alias rejection ≥ 80 dB (worst 86.79 dB)

Output

- 16-bit complex I/Q and 32-bit packed {Q, I} word
- Convergent rounding, saturation and overrange flag
- Gain 0 dB or +6.02 dB
- Raw four-lane ADC bypass with 3-cycle latency

Control and Integration

- Atomic commit of five shadow settings by one strobe
- Accept / defer / reject arbitration; busy and sticky error flags
- 4-bit epoch tag; deterministic multi-device phase sync
- Power-down with deferred commit; input pause without sample loss
- Single clock domain; reset with 3-stage synchronized release; scan test inputs

Applications

Direct RF and IF sampling receivers, software-defined radio, phased-array radar and electronic warfare receivers, wireless infrastructure and test and measurement front ends.

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