PHOENIX-DUC

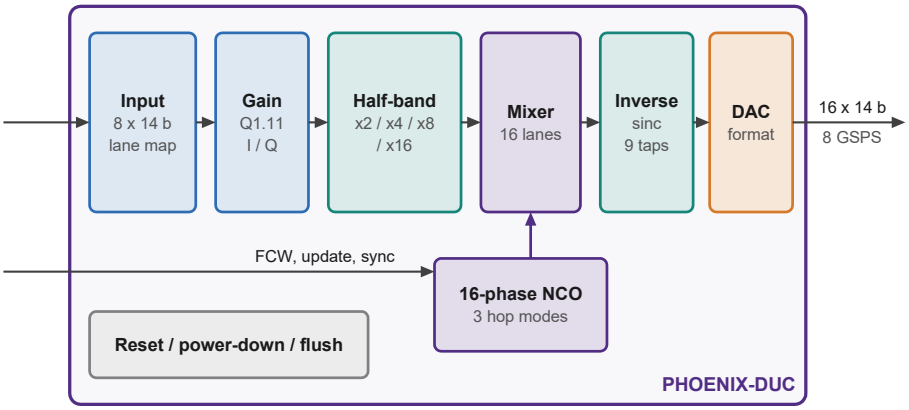
8 GSPS Multi-Mode Digital Up-Converter with 16-Phase CORDIC NCO

PHOENIX-DUC delivers an 8 GSPS aggregate DAC stream on 16 parallel output lanes from one 500 MHz functional clock. Eight shared input lanes support 2×, 4×, 8× and 16× interpolation through four 55-tap half-band stages.

The 32-bit, 16-phase CORDIC NCO has a 1.862645 Hz grid, a shadow word with commit / acknowledge, and reset, continuous and coherent hop modes; synchronized SYSREF events set the phase-time origin. Every combination of retune, alignment, mode change and power-down has one defined result. Quadrature mixing is available in 4×, 8× and 16×.

Q1.11 gain and a 9-tap inverse-sinc FIR compensate the DAC hold droop with 0.029715 dB error over 0..0.4 fDAC; invalid output cycles drive the 14-bit offset-binary mid-scale code.

Block Diagram



Implementation Results

Delivered configuration, default widths; setup WNS = 0.00 ns at clk_i = 500 MHz.

Target	Technology	Area / Resources
ASIC	TSMC 28nm HPC+	307,126.5 µm² · 812.5k gates
FPGA	AMD Virtex UltraScale+	32,107 LUTs · 30,670 FFs · 548 DSPs

ASIC: logic synthesis, ssg 0.81 V / 125 C, pre-layout, ideal clock; gates in NAND2 equivalents (0.378 µm²), no single- / dual-port memories. FPGA: synthesis for xcvu9p-flga2104-2-e (out of context), 0 BRAM, post-synthesis WNS = -9.651 ns at 2.00 ns. Contact SILIPRISM for results on your technology.

Verification

Simulation: all 157 test cases pass, 155 by exact sample comparison with the fixed-point math model (tolerance 0); in every test case a port-level cycle checker checks valid, acknowledge, busy, error and the 16 lane phases with 0 mismatches; the block-level NCO event matrix gives 0 errors. Math model: all specification checks pass. Code coverage: line 97.89%, branch 94.30%, toggle 94.80%, condition 78.35%. Lint 0 errors; CDC / RDC 0 errors, 0 warnings; the synthesis netlist is proven equivalent to the RTL.

Deliverables

- Synthesizable Verilog-2001 RTL source
- Timing constraints; ASIC and FPGA synthesis scripts
- Lint, CDC and RDC setup with constraints and waivers
- Top-level testbench, port-level and NCO checkers, 157 test configurations, math models
- SoC CSR wrapper contract and C99 programming reference (document)
- Specification, programming guide and verification report

FEATURES

Signal Processing

- Selectable 2×, 4×, 8×, 16× interpolation
- 55-tap half-band stages: ripple ≤ 0.000928 dB, stopband ≥ 89.49 dB
- Q1.11 digital gain for back-off and PAPR control
- 9-tap inverse-sinc DAC droop equalizer

NCO & Modulation

- 16-phase 32-bit CORDIC NCO, 1.862645 Hz step
- Reset, continuous and coherent hop modes
- Shadow word with commit / acknowledge
- SYSREF-triggered phase-origin alignment
- One carrier event per clock edge, defined result

DAC Interface

- 16 lanes x 14-bit offset binary, 8 GSPS
- All-lane clip flag; mid-scale mute when idle
- Configuration and command status outputs

Integration

- One 500 MHz functional clock, no internal clocks
- Self-flushing interpolation change
- Power-down with state retention; 2-stage sync
- 3-stage reset release; scan / test enables

Applications

Wireless transmitters, phased-array radar exciters, direct digital RF synthesis and multi-channel waveform generators.

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