PHOENIX-FLEXRAY

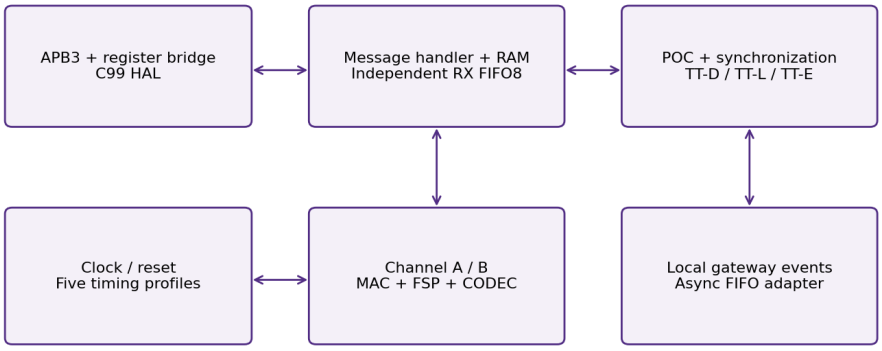
Dual-Channel FlexRay 3.0.1 Communication Controller

PHOENIX-FLEXRAY is a high-reliability, synthesizable Verilog-2001 IP core fully compliant with the FlexRay Communications System Protocol Specification v3.0.1. It delivers deterministic, fault-tolerant, and high-bandwidth in-vehicle networking for safety-critical automotive electronic control units (ECUs), including ADAS domain controllers, steer-by-wire, brake-by-wire, chassis dynamics, powertrain management, and central vehicle gateways. The core supports distributed time-triggered (TT-D), locally synchronized (TT-L), and externally synchronized (TT-E) operation on channel A, channel B, or dual-channel redundant topologies at 2.5, 5.0, and 10.0 Mbit/s.

At the protocol layer, the engine implements the complete FlexRay 3.0.1 state machinery and execution processes. It features fault-tolerant clock synchronization supporting up to 15 sync frame pairs via the Fault-Tolerant Midpoint (FTM) algorithm, dual key slot coldstart transmission, flexible static segment arbitration and dynamic minislotting, symbol window transmission (CAS/MTS), and Network Idle Time (NIT) processing. Physical layer coding and decoding incorporate bit strobing with 8/10-sample majority voting, Wakeup Pattern (WUP/WUDOP) decoding, channel idle detection, 11-bit header CRC, and 24-bit frame CRC verification.

Host software interfaces through an AMBA 3 APB (APB3) slave port with robust request/acknowledgement CDC handshakes. The subsystem provides configurable 2 to 128 message buffers within an 8 KB to 128 KB synchronous message RAM, an independent 8-entry dedicated receive FIFO (up to 254 bytes payload per entry) with atomic multi-field filter commitment, two absolute macrotick/cycle timers (T0C/T1C), atomic buffer locking, seven synchronized interrupt outputs, and a 12-byte Network Management Vector (NMV). An ordered asynchronous time gateway enables deterministic cross-clock timebase forwarding without receiver backpressure.

Block Diagram



Implementation Results

Synthesis results at 80 MHz protocol clock (fr_clk) and 100 MHz APB host clock (apb_clk). Default configuration: MB_NUM = 64, MRAM_DEPTH = 2048 words (8 KB), RST_SYNC_STAGES = 3.

Configuration / Technology	Clock Target	Area / Resources / Timing
Dual-Channel Core · TSMC 28nm HPC+	80 MHz / 100 MHz	319,765 µm² · 846k gates · WNS +3.78 ns
Dual-Channel Core · AMD Virtex UltraScale	80 MHz / 100 MHz	11,686 LUTs · 8,167 FFs · 2 RAMB36 · +5.94 ns
Time Gateway Core · TSMC 28nm HPC+	100 MHz / 100 MHz	2,418 µm² · 6.4k gates · WNS +5.12 ns

ASIC: Design Compiler, ssg 0.72V 125°C, 1 gate = ND2D1 (0.378 µm²). FPGA: Vivado synthesis, xcvu440-3. All timing closed with positive slack. Contact SILIPRISM for results on your target technology.

Verification

Verified across 23 independent directed testbenches (100% PASS), a 15-test UVM cluster regression with APB and FlexRay VIP across 5 random seeds (100% PASS), and a 342-vector / 1,026-assertion C99 driver co-simulation oracle. Signoff covers MRAM dense lock budget, POC second CCF collision recovery, 15 sync frame pairs FTM convergence, and TT-E recovery edges.

Signoff results: 100% protocol and functional coverage, ≥95% code coverage (statement, branch, condition, toggle, and FSM). Multi-node strict C99 compiler signoff (-std=c99 -Wall -Wextra -Wpedantic -Wconversion -Werror) passes clean. SpyGlass static signoff reports 0 fatal, 0 error, and 0 CDC/RDC warnings; Formality RTL-to-netlist LEC and DFT scan DRC clean.

Deliverables

- Synthesizable Verilog-2001 RTL source (31 core modules) and technology-independent wrappers
- SDC timing constraints, Design Compiler and Vivado synthesis scripts
- SpyGlass lint, CDC and RDC rule scripts with audited waiver manifests and review reports
- UVM verification environment, testbench suite, and 23 independent directed testbenches
- C99 bare-metal driver with HAL API, reference examples, and co-simulation testbenches
- Comprehensive documentation: Hardware Specification, Programming Guide, Verification Guide
- Contact SILIPRISM for additional delivery options, technical support, and customization

FEATURES

FlexRay 3.0.1 Protocol

- Full compliance with Protocol Specification v3.0.1
- TT-D, TT-L and TT-E operating modes
- 2.5, 5.0 and 10.0 Mbit/s bus data rates
- All five Table B-16 sample/microtick profiles
- Dual-channel (A & B) or single-channel operation
- Two key slots support; WUDOP wakeup pattern
- 11-bit header CRC and 24-bit frame CRC
- FTM clock synchronization up to 15 sync frames

Deterministic MAC & Coding

- Configurable static segment & dynamic minislotting
- Symbol window (CAS/MTS) and Network Idle Time (NIT)
- Action point offsets and channel idle delimiter
- Bit strobing with 8/10x majority voting & glitch rejection
- Low-power wakeup pattern and channel idle detection

Host Interface & Message RAM

- AMBA 3 APB (APB3) slave, 32-bit register access
- Configurable 2 to 128 message buffers
- Flexible 1024 to 32768 words synchronous message RAM
- Independent 8-entry RX FIFO (up to 254B payload/entry)
- Atomic FIFO filter commit (channel, FID, cycle, MID)
- Hardware buffer enable and atomic lock mechanism
- Two absolute macrotick/cycle timers (T0C and T1C)
- Seven synchronized interrupt outputs and 12-byte NMV

Time Gateway & Reliability

- Ordered 8-entry asynchronous time gateway FIFO
- Signed 32-bit rate and offset correction transfer
- Zero receiver backpressure to source protocol
- Asynchronous release synchronizers (≥ 3 stages)
- DFT scan bypass mode (test_mode_i)

Software Support

- C99 MISRA-compliant bare-metal driver with HAL API
- Host, ARM Cortex-M, and RTL co-simulation verification
- Step-by-step worked examples and porting guide

Applications

Automotive ADAS domain controllers, steer-by-wire, brake-by-wire, powertrain management, active suspension, central vehicle gateways, safety-critical industrial robotics, and fault-tolerant distributed control networks.

Contents subject to change without notice.
Trademarks are the property of their respective owners.