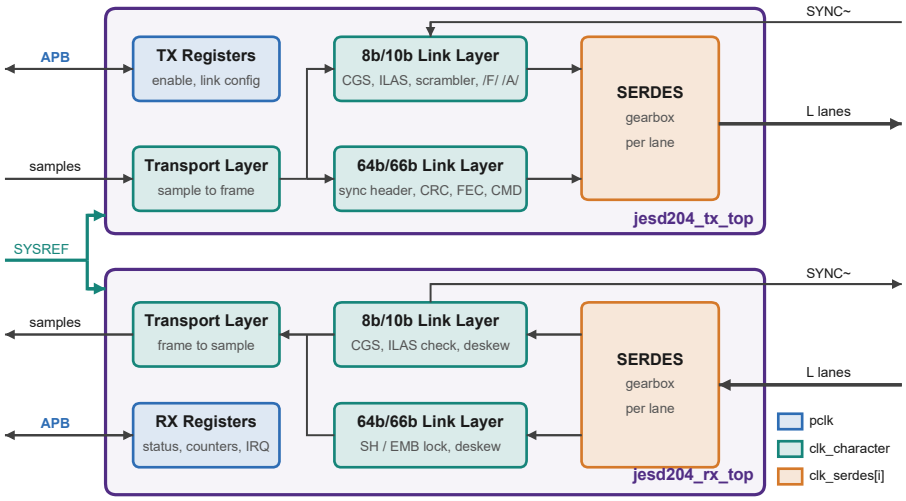
PHOENIX-JESD204BC

JESD204B / JESD204C Transmit and Receive Controller

PHOENIX-JESD204BC is a JESD204B.01 and JESD204C serial interface controller for high-speed data converters. The transmitter maps converter samples into frames for DAC links; the receiver recovers the frames of ADC links and de-maps them into samples. Both cores carry the 8b/10b (JESD204B) and the 64b/66b (JESD204C) link layer, selected before the link is enabled, and support up to 24 lanes and 96 converters.

The cores connect to any SERDES PHY through a per-lane parallel interface of 20, 40 or 80 bits, handle subclass 0, 1 and 2 deterministic latency with SYSREF and SYNC~, and are configured by software through an APB register bus. Lane deskew, frame replay and transport framing use external dual-port RAMs, so memory BIST stays in the SoC.

Block Diagram



Implementation Results

Delivered configuration: both link layers, default parameters (TX L = 2, RX L = 4, M = 10, SERDES width 40).

Target	Technology	TX core	RX core
ASIC	TSMC 28nm HPC+	295.9 k gates	1,654.9 k gates
FPGA	AMD Virtex UltraScale+ xcvu13p-fhgb2104-2-i	181,477 LUT · 18,097 FF	188,479 LUT · 101,775 FF
Slack	ASIC / FPGA setup	+0.780 / +0.732 ns	+0.490 / +3.934 ns

ASIC: ssg 0.81 V 125 °C, pre-layout cell area 111,838 / 625,564 µm² (TX / RX), 1 gate = 0.378 µm² (NAND2), setup met at clk_character 363.64 MHz and clk_serdes 375 MHz. FPGA: place and route, timing met at pclk 100 MHz, clk_character / clk_sample 75 MHz, clk_serdes 100 MHz. External RAMs not included.

Verification

Verified in a UVM environment against a JESD204 VIP (transmit and receive device) and an APB VIP: 106 / 106 regression cases pass, covering 8b/10b and 64b/66b, SERDES widths 20 / 40 / 80, 1 to 24 lanes, subclass 0 / 1 / 2, control words and the link test patterns. Synthesis netlists are proven equivalent to the RTL. Lint, CDC and RDC setups are delivered for SoC-level sign-off.

Deliverables

- Synthesizable Verilog-2001 RTL, build-time configuration macros
- SDC constraints; ASIC and FPGA synthesis scripts
- Lint, CDC and RDC setup with constraints and waiver file
- UVM testbench with regression lists (JESD204 and APB VIP licensed separately)
- Specification, programming guide with C99 reference code and verification guide, in Chinese and English
- Behavioral model of the external dual-port RAM for simulation and FPGA

FEATURES

JESD204B / JESD204C

- JESD204B.01 8b/10b and JESD204C 64b/66b link layers, one or both built in
- 1 to 24 lanes, 1 to 96 converters, F up to 256, S up to 8
- N up to 32, N' 8 to 32, CS 0 to 3, CF 0 / 1, HD 0 / 1
- Subclass 0, 1 and 2 (2: 8b/10b), SYSREF window, ignore and force

Deterministic Latency

- SYSREF position counters, software SYSREF
- Programmable receive buffer release point

8b/10b Link Layer

- CGS, ILAS generation and checking
- Scrambling, /F/ and /A/ character replacement
- SYNC~ error reporting, frame replay
- Link test: PRBS-15, JTSPAT, JSPAT, K28.5, D21.5, K28.7
- Software SYNC request, error injection

64b/66b Link Layer

- Sync header and extended multiblock lock
- CRC-12, CRC-3, FEC and command channel options
- Programmable lock thresholds, per-lane error reports
- Scrambler 1 + x^39 + x^58
- 64-bit data bit order selection

Transport Layer

- Mappers for small (F < 8) and big (F ≥ 8) frames
- Short and long transport layer test patterns

Test and Status

- Per-lane link test receive counters
- Read-to-clear status counters, maskable interrupt

Integration

- SERDES interface 20 / 40 / 80 bits per lane
- Sample interface with 1:1 to 1:8 clock ratio, up to 32 samples per converter per clock
- AMBA 3 APB register bus, pclk
- External deskew, replay and framing RAM ports
- Active-high resets with synchronous release, scan mode

Applications

High-speed ADC and DAC links in wireless base stations, radar, test and measurement instruments, medical imaging and software-defined radio.

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