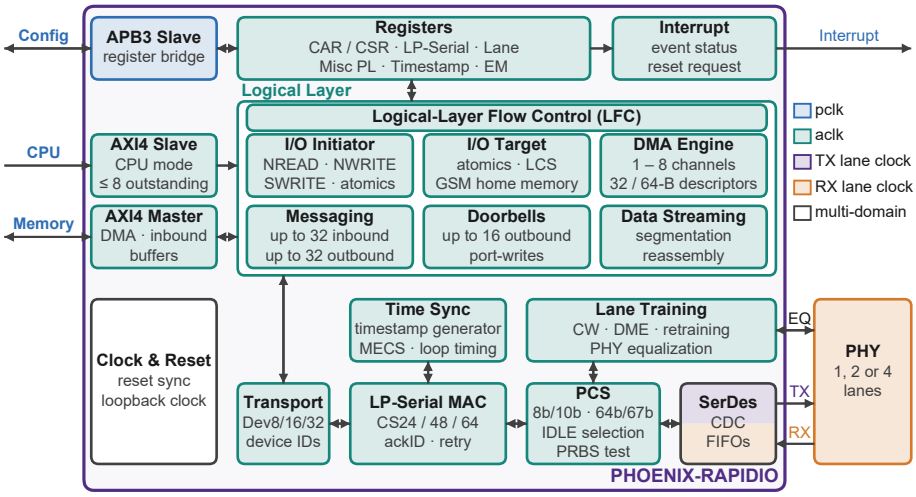
PHOENIX-RAPIDIO

RapidIO 4.1 Serial Endpoint Controller up to 25.78125 Gbaud

PHOENIX-RAPIDIO is a RapidIO 4.1 serial endpoint controller IP core, delivered as synthesizable Verilog-2001 RTL. It connects an SoC to one 1x, 2x or 4x LP-Serial port through a SerDes PHY that only serializes and deserializes; coding, deskew, port initialization, lane training, the link protocol, the transport and logical layers, DMA and the registers are inside the core. Lanes run at five 8b/10b rates from 1.25 to 6.25 Gbaud (IDLE1, IDLE2) and at 10.3125, 12.5 and 25.78125 Gbaud with 64b/67b (IDLE3), the IDLE sequence selected automatically or forced by software; 64b/67b links use long-run lane training with a per-lane PHY equalization interface.

Control symbols CS24, CS48 and CS64 carry ackID acknowledgment, retry, error recovery and flow control, and synchronize time: multicast events (MECS), timestamp sequences and loop timing keep the 64-bit timestamp generators of a system aligned. The logical layers cover I/O with atomics, maintenance, port-writes, doorbells, messages, GSM home operations, data streaming, flow control and error management with 8-, 16- and 32-bit device IDs and 34-, 50- and 66-bit addresses. Software uses an APB3 slave and the included HAL 2.0 C driver; the AXI4 master serves the DMA engine (atomics, 32- or 64-byte descriptors), the inbound target and the message buffers, and the AXI4 slave turns CPU accesses in outbound windows into RapidIO requests (up to eight outstanding, atomics included). PRBS lane tests with internal or PHY loopback check every lane.

Block Diagram



Implementation Results

Build	Technology	Area / Resources	Clock · WNS (ns)
4 lanes × 80 bit	TSMC 28nm HPC+	821,406 µm² · 905.3 k gates	625 MHz · 0.0001
1 lane × 20 bit	TSMC 28nm HPC+	722,153 µm² · 664.5 k gates	625 MHz · −0.0000
4 lanes × 80 bit	AMD Virtex UltraScale	123,071 LUTs · 67,938 FFs · 20 BRAM	200 MHz · −1.596
1 lane × 20 bit	AMD Virtex UltraScale	80,882 LUTs · 54,872 FFs · 20 BRAM	200 MHz · −1.548

Both builds with 256-bit AXI and all other parameters at their defaults. ASIC: Synthesis, BWP30P140 RVT + HVT cells, SSG 0.81 V 125 °C; aclk 625 MHz (1.6 ns), SerDes word clocks 0.775 ns, pclk 200 MHz; WNS is the worst aclk setup slack of pre-layout static timing analysis of the synthesized netlist, timing closure after place and route is an SoC integration acceptance requirement; aclk logic depth 47.5 ND2 delay equivalents (limit 50). Gate count in NAND2 equivalents (0.378 µm²), excluding the single-port / dual-port memories implemented as register models; area is the logic area plus 50% of the register-model area of those memories. The memories are delivered as register models and can be replaced by SRAM macros at SoC integration: inbound packet buffer 512 × 256 (128 Kbit); retransmit buffer 512 × 256 (128 Kbit); I/O target read buffer 64 × 256 (16 Kbit); DMA payload buffer 64 × 256 (16 Kbit); message payload buffer 64 × 256 (16 Kbit); CPU-mode response buffer 32 × 256 (8 Kbit); outbound queue lists 2 × 256 × 14 (7 Kbit); SerDes TX FIFO 16 × 320 (5 Kbit); message completion queue 64 × 52 (3.25 Kbit); DMA TID address table 64 × 48 (3 Kbit); SerDes RX FIFO 4 × 8 × 80 (2.5 Kbit); port-write queue 4 × 295 + 4 × 256 (2.15 Kbit); total 334.9 Kbit (1-lane build: SerDes TX FIFO 16 × 80, SerDes RX FIFO 8 × 80; total 329.3 Kbit). FPGA: FPGA synthesis, xcvu440-flgb2377-3-e, out of context, 1 DSP; WNS is the worst slack at the 5 ns aclk constraint.

Verification Summary

UVM environment with in-house APB3 and AXI4 models; ports run in loopback, back to back or against a RapidIO link-partner model through a channel model with per-lane skew, ppm offset, polarity inversion, lane loss, bit errors and PHY equalization. All 574 regression runs on 15 builds pass, including the 12 lane-count × SerDes-width builds, all eight lane rates, lane training, time synchronization, latency and random tests; 19 block benches pass.

Code coverage of the default build (170 runs; reviewed waivers and formally unreachable items excluded), measured / target in %: line 98.64 / 98, branch 97.18 / 95, condition 93.09 / 90, toggle 90.96 / 90, FSM states 100 / 100, FSM transitions 97.07 / 95. Lint: 0 errors. CDC, RDC: 0 errors. Equivalence verification of both netlists against RTL: 0 failing, aborted or unverified points. HAL 2.0 driver: host unit test, Cortex-M4 build without warnings, RTL co-simulation (5,767 APB transfers), all passing.

Deliverables

- Synthesizable Verilog-2001 RTL with technology-cell and memory wrappers
- Register map (CSV) with generated UVM register model and C header
- HAL 2.0 C99 driver: host unit tests, Cortex-M build, RTL co-simulation tests
- UVM testbench with bus, channel and link-partner models, regression lists
- Synthesis constraints and scripts; Lint, CDC, RDC and equivalence scripts
- Specification, programming guide, verification report and brief, Chinese and English

FEATURES

RapidIO 4.1 Physical Layer

- 1x, 2x or 4x LP-Serial port; SerDes word of 20, 40, 64 or 80 bits per lane
- 8b/10b at 1.25, 2.5, 3.125, 5 and 6.25 Gbaud (IDLE1, IDLE2)
- 64b/67b at 10.3125, 12.5 and 25.78125 Gbaud (IDLE3), up to 103.125 Gbaud per port
- Automatic IDLE sequence selection or software-forced IDLE1 / IDLE2 / IDLE3
- Long-run 64b/67b lane training: codeword (CW) and DME training, retraining
- Per-lane PHY transmit / receive equalization request-acknowledge interface
- Lane deskew; automatic polarity detection with IDLE2, per-lane software polarity inversion otherwise

Link Layer

- CS24 / CS48 / CS64 control symbols
- ackID acknowledgment, retry, link error recovery, reset-port and reset-device
- Receiver- and transmitter-controlled flow control; four priorities and CRF
- Retransmit and inbound buffers of 8 to 64 packets; cut-through transmit
- TX / RX latency 34.2 / 19.1 ns (25.78125 Gbaud)

Time Synchronization

- 64-bit timestamp generator with fractional-ns step
- MECS send and receive: register command, pin or periodic master ticks
- Timestamp sequences and loop-timing delay measurement

Transport and Logical Layers

- Dev8, Dev16 and Dev32 device IDs; 34-, 50- and 66-bit addresses
- NREAD, NWRITE, NWRITE_R, SWRITE, maintenance, LCS window
- Atomics as initiator (DMA, CPU mode) and target (AXI exclusive accesses)
- Messages: up to 32 inbound engines bound to mailboxes 0–63, up to 32 outbound engines
- Doorbells: up to 16 parallel outbound slots, inbound FIFO; inbound port-writes up to 64 bytes
- Data streaming segmentation and reassembly; a stream uses one DMA channel at a time
- GSM home memory operations without directory; coherence managed by software
- Logical-layer flow control: 8-entry stopped-flow table, 8-entry controlled-flow list; each DMA channel and outbound message engine stops on its own flow
- Error management: capture, error-rate thresholds, port-write notification

SoC Integration

- AXI4 master: DMA with 1 to 8 channels, 32- or 64-byte descriptor chains; up to 128 DMA requests awaiting a RapidIO response
- AXI4 slave: CPU mode through 1 to 16 outbound windows, up to 8 outstanding requests
- 1 to 16 inbound windows; AXI data 64 / 128 / 256 bits, address 32 to 64 bits
- APB3 slave for all CAR / CSR and extended feature blocks
- Level interrupt, reset-device request, MECS and timestamp outputs
- Independent AXI, APB and SerDes clocks

Test and Debug

- PRBS7 to PRBS31 lane test with error counters and error injection
- Internal and PHY loopback: lane self-test without a link partner
- Raw packet transmit and receive; receive error injection
- Scan test mode with pin-controlled domain resets

Applications

Chip-to-chip and backplane fabrics in wireless infrastructure, defense and aerospace, high-performance computing and embedded systems, including base-station and radar systems that need system-wide time synchronization.

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